



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,783	09/16/2003	Hui Wang	495152000610	4793
7590	12/16/2004			EXAMINER ESTRADA, MICHELLE
Peter J. Yim Morrison & Foerster LLP 425 Market Street San Francisco, CA 94105-2482			ART UNIT 2823	PAPER NUMBER

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,783	WANG ET AL.	
	Examiner	Art Unit	
	Michelle Estrada	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 27 August 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 11-60 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 31-43 is/are allowed.

6) Claim(s) 11,15,16,21-24,28-30,44,47,48,52-55 and 58-60 is/are rejected.

7) Claim(s) 12-14,17-20,25-27,45,46,49-51,56 and 57 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>10/30/03</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Claims 11-43 in the reply filed on 8/27/04 is acknowledged.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 10/30/03 have been considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 11, 15, 24 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Reid (6,653,226).

With respect to claim 11, Reid discloses a dielectric layer (103) formed on a semiconductor wafer (101) having a recessed area and a non-recessed area (See Fig. 1A); a plurality of dummy structures formed within the recessed area, wherein the dummy structures are inactive areas configured to increase the

Art Unit: 2823

planarity of a metal layer (105) subsequently formed on the dielectric layer; a metal layer (105) formed to fill the recessed area and cover the non-recessed area and the plurality of dummy structures (See Fig. 1A), wherein the metal layer is electropolished to expose the non-recessed area (See Fig. 1B) (Col. 1, lines 50-57).

With respect to claim 15, Reid discloses wherein the metal layer is formed by depositing the metal layer (Col. 1, lines 54-55).

With respect to claim 24, Reid discloses wherein the recessed area is a wide trnch configured to form an interconnection when filled with the metal layer (Col. 1, lines 15-16).

With respect to claim 29, Reid discloses wherein the plurality of dummy structures includes the same material as the dielectric layer (Col. 1, lines 50-52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any

inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 16, 21-23, 28, 44, 47, 48, 52-55, 58, 59 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reid as applied to claims 11, 15, 24 and 29 above, and further in view of Cox (6,383,917).

Reid does not disclose wherein the metal layer is formed by electroplating the metal layer; the structure further comprising a barrier layer formed on the dielectric layer before forming the metal layer; a cover layer formed on the semiconductor wafer after electropolishing the metal layer; where the metal layer is copper.

With respect to claim 16, Cox discloses forming a metal layer (105) by electroplating (Col. 3, lines 58-60).

With respect to claim 21, Cox discloses further comprising a barrier layer (104) formed on the dielectric layer (103) before forming the metal layer (Col. 3, lines 19-21).

With respect to claim 22, Cox discloses further comprising a seed layer formed on the dielectric layer before forming the metal (Col. 3, lines 58-60).

With respect to claim 23, Cox discloses a cover layer (107/109) formed on the semiconductor wafer after electropolishing the metal layer.

With respect to claim 28, Cox discloses wherein the metal layer (105) is copper (Col. 3, lines 35-43).

With respect to claim 30, Cox discloses wherein the plurality of dummy structures includes a metal (Col. 4, lines 48-60).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Reid and Cox to enable the process of Reid to be performed according to the process of Cox because electroplating is inexpensive, fast and effective for thick layers, forming a barrier layer in Reid will prevent diffusion of the metal layer, forming a seed layer is typically done when performing electroplating, forming a cover layer will provide protection to the structure, and the formation of dummy metal regions to the structure increase the surface area of the conductive material thus optimizing the process account for these changes in local fields, which could affect the uniformity of the etch rate.

With respect to claim 44, Reid does not disclose wherein the metal layer is overpolished to allow the non-recessed area to protrude past a surface of the metal layer in the recessed area. Cox discloses wherein the metal layer (105) is overpolished to allow the non-recessed area to protrude past a surface of the metal layer in the recessed area (See Fig. 1c and Col. 4, lines 1-14).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Reid and Cox to enable the electropolishing of Reid to be performed according to the teachings of Cox because the overpolishing enables production of an integrated circuit that maintains the strength characteristics imparted by the dielectric layer.

With respect to claim 47, Reid discloses wherein the metal layer is formed by depositing the metal layer (Col. 1, lines 54-55).

With respect to claim 48, Cox discloses forming a metal layer (105) by electroplating (Col. 3, lines 58-60).

With respect to claim 52, Cox discloses further comprising a barrier layer (104) formed on the dielectric layer (103) before forming the metal layer (Col. 3, lines 19-21).

With respect to claim 53, Cox discloses further comprising a seed layer formed on the dielectric layer before forming the metal (Col. 3, lines 58-60).

With respect to claim 54, Cox discloses a cover layer (107/109) formed on the semiconductor wafer after electropolishing the metal layer.

With respect to claim 55, Reid discloses wherein the recessed area is a wide trench configured to form an interconnection when filled with the metal layer (Col. 1, lines 15-16).

With respect to claim 58, Cox discloses wherein the metal layer (105) is copper (Col. 3, lines 35-43).

With respect to claim 59, Reid discloses wherein the plurality of dummy structures includes the same material as the dielectric layer (Col. 1, lines 50-52).

With respect to claim 60, Cox discloses wherein the plurality of dummy structures includes a metal (Col. 4, lines 48-60).

Allowable Subject Matter

Claims 12-14, 17-20, 25-27, 45, 46, 49-51, 56 and 57 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: there is no disclosure in the prior art, either alone or in combination of the limitations recited in claims 12-14, 17-20, 25-27, 45, 46, 49-51, 56 and 57.

Claims 31-43 are allowed.

The following is an examiner's statement of reasons for allowance: With there is no disclosure in the prior art of electropolishing the barrier layer deposited on the non-recessed area, and wherein the exposed barrier layer is removed at a first rate and the non-recessed area of the dielectric layer is removed at a second rate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Estrada whose telephone number is 571-272-1858. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2800.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Michelle Estrada

Examiner

Art Unit 2823

ME

December 13, 2004